REMARKS/ARGUMENTS

Claims 1-61 are pending in the application, and claims 25-36 and 55-61 are withdrawn. The Applicants' attorney has amended claims 1, 48, 53. As discussed below, all of the claims are in condition for allowance. **But if after considering this response the Examiner does not allow all of the claims, then the Applicants' attorney requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Objections To The Specification

The Applicants' attorney believes that the amended title of the application submitted in a response filed 19 December 2007 is descriptive of the claimed invention. If the Examiner continues to disagree, he is requested to propose a new title.

Objection To The Claims

The Applicants' attorney has amended claims 48 and 53 as proposed by the Examiner, and, therefore, requests the Examiner to withdraw this objection.

Rejection Of Claims 10-18 Under 35 U.S.C. § 112 First Paragraph

In general, an embodiment covered by claims 10 and 18 provide for buffering of data between portions (*e.g.*, threads) of a software application.

Support for claim 10 is found in FIG. 5 and paragraph [82] of the patent application.

Support for claim 18 is also found in FIG. 5 and paragraph [82], and in, *e.g.*, paragraph [69], which describes how the data-transfer objects 86_b may package the generated data into a message that includes a header and the data.

Claims 11-17 are also supported by the specification as implied by the Examiner.

Rejection Of Claims 1-3, 5-12, and 14-15, 17-18, 37, 39-43, 45, and 47-49 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 4,703,475 To Dretzka

Claim 1

Claim 1 as amended recites a processor operable to load at least a portion of published data into the first buffer and to load at least the same portion of the published data into the second buffer that is parallel to the first buffer.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [67] – [72] and [83] of the patent application, in an embodiment, a processor 42 is operable, under the control of an application thread 100_3, to publish data, and is operable, under the control of data-transfer object 86_{3a}, to load at least a portion of the published data into a first buffer 106_3, and is operable, under the control of data-transfer object 86_{5a}, to load at least the same portion of the published data into a second buffer 106_5, which is parallel to the first buffer.

In contrast, Dretzka does not disclose a processor operable to load at least a portion of published data into the first buffer and to load at least the same portion of the published data into the second buffer that is parallel to the first buffer. Referring, *e.g.*, to Dretzka's FIGS. 1 and 5, a processor 11 loads a same portion of published data into only a single buffer 120, not into multiple buffers 120. And the data in the single buffer 120 is transferred to only a corresponding single buffer 130. A similar analysis applies to the buffers 220 and 230 of FIG. 6. And referring, e.g., to FIGS. 7-11, even if the Examiner incorrectly believes that the links 40 are equivalent to the buffers recited in claim 1, there is no same portion of published data that is loaded onto more than one of these links. For example, packets 1 and 6 are loaded only onto link 40-4, packets 2 and 7 are loaded only onto link 40-3, packets 3 and 8 are loaded only onto link 40-2, packet 4 is loaded only onto link 40-1, and packet 5 is loaded only onto link 40-0.

Claims 2-3 and 5-9

These claims are patentable by virtue of their respective dependencies from claim 1.

Claim 10

Claim 10 as amended recites a processor operable to generate data under the control of an application, load the data into a buffer, unload the data from the buffer, and process the unloaded data under the control of the application.

For example, referring, e.g., to FIGS. 3-5 and paragraph [82] of the patent application, in an embodiment, a processor 42 is operable to generate data under the control of a first thread 100_3 of an application 80, load the data into a buffer 106_5 under the control of a data-transfer object 86_{5a}, unload the data from the buffer 106_5 under the control of a second data-transfer object 86_{5b}, and process the unloaded data under the control of a second thread 100_4 of the same application 80.

In contrast, Dretzka does not disclose a processor operable to generate data under the control of an application, load the data into a buffer, unload the data from the buffer, and process the unloaded data under the control of the application. Referring, e.g., to Dreztka's FIGS. 1 and 5, a processor 11 arguably generates data under the control of an application, loads the data into a buffer 120, and unloads the data from the buffer. But Dreztka does not disclose that the processor 11 then processes the unloaded data under the control of the application; Dreztka discloses only that another processor 21 processes the unloaded data, arguably under the control of another application. A similar analysis applies to the processor 21.

Claims 11-12, 14-15, and 17-18

These claims are patentable by virtue of their respective dependencies from claim 10.

Claim 37

Claim 37 recites publishing, with an application, data that includes no information indicating a destination of the data.

For example, referring, *e.g.*, to FIGS 3-5 and paragraphs [66] – [70] of the patent application, in an embodiment a thread 100_1 of an application 80 publishes data that includes no information indicating a destination of the data, and a data-transfer object 86_{1a} loads the published data into a buffer 106_1. Because the channel 104_1 corresponds to a single destination, another data-transfer object 86_{1b} adds to the published data information (*e.g.*, a header) indicating a destination of the published data. This relieves the application 80 and thread 100_1 of the burden of adding destination information to the published data.

In contrast, Dretzka does not disclose publishing, with an application, data that includes no information indicating a destination of the data. Referring, e.g., to FIGS. 2 and 5 and col. 7, lines 25-30, and col. 8, lines 51-58, Dretzka's processor 11 (arguably an application running on the processor) publishes a message that includes information (e.g., message sequence numbers) indicating a destination of the data. The processor 11 must including this destination information with the message, because any available logical channel LCN may carry any message. That is, no logical channel LCN is associated with a predetermined destination. Therefore, if the processor 11 does not include destination information with the message, then the system will not know where to send the message.

Claims 39-43

These claims are patentable by virtue of their respective dependencies from claim 37.

Claim 45

Claim 45 recites receiving a message that includes data and that includes a message header that indicates a destination of the data, and loading into a buffer the

received data without the message header, the buffer corresponding to the destination.

For example, referring, e.g., to FIGS. 3-5 and paragraphs [76] – [77], in an embodiment a communication object 88 receives from a pipeline bus 50 a message that includes data and that includes a message header that indicates a destination of the data. A data-transfer object 86_{2b} strips the message header from the message and loads the data (without the stripped message header) into a buffer 106_2 that corresponds to the application threads 100_1 and 100_2, which are the destinations of the data.

In contrast, Dretzka does not disclose loading into a buffer received data without a message header, the buffer corresponding to a destination of the data. Referring, e.g., to FIGS. 5-6 and col. 8, line 47 – col. 10, line 24, Dretzka loads the queues and buffers 110, 120, 130, 230, 220, and 210 only with received messages that each include a message header that indicates a destination of the data within the respective message. Furthermore, because Dretzka's logical channels LCN are selectable for any message based on availability, none of Dretzka's queues or buffers does or can correspond to a destination of the data with which it is loaded.

Claims 47-49

These claims are patentable by virtue of their respective dependencies from claim 45.

Rejection Of Claims 4, 13, 38, 44, 46, And 50 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of The Examiner's Taking Of Official Notice

Claim 4

Claim 4 is patentable by virtue of its dependency from claim 1.

Claim 13

Claim 13 is patentable by virtue of its dependency from claim 10.

Claims 38 and 44

These claims are patentable by virtue of their dependencies from claim 37.

Claims 46 and 50

These claims are patentable by virtue of their dependencies from claim 45.

Rejection Of Claims 19-24 and 51-54 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of U.S. Patent 6,216,191 to Britton

Claim 19

Claim 19 recites a pipeline accelerator that includes a destination of data and that is operable to receive a message that includes information indicating the destination, to recover the data from the message, and to process the recovered data at the destination without executing a program instruction.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [67] – [72] of the patent application, in an embodiment, a processor 42 constructs a message that includes data and information indicating a destination of the data within a pipeline accelerator 44, and drives the message onto a bus 50. The accelerator 44 is operable to receive the message from the bus 50, to recover the data from the message, and to process the recovered data at the destination without executing a program instruction.

In contrast, neither Dreztka nor Britton, viewed alone or in combination, discloses a pipeline accelerator that includes a destination of data and that is operable to receive a message that includes information indicating the destination, to recover the data from

the message, and to process the recovered data at the destination without executing a program instruction.

The Examiner admits on p. 26 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.,* to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to receive a message that includes information indicating a destination of data and to recover data from the message. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA having an address-bus/data-bus interface and lacking a message-based interface as recited in claim 19, the Examiner has failed to make a prima facie showing of obviousness.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 19.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 19 obvious.

Claims 20-21

These claims are patentable by virtue of their dependencies from claim 19.

Claim 22

Claim 22 recites a pipeline accelerator operable to generate data without

executing a program instruction, to generate a header including information indicating a destination of the data, and to package the data and header into a message.

Referring, *e.g.*, to FIG. 3, paragraph [49], and paragraph [74] of the patent application, a pipeline accelerator 44 is operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data (e.g., a thread 100 of an application program 80 of FIG. 5), to package the data and header into a message, and to drive the message onto a bus 50.

In contrast, neither Dretzka nor Britton, viewed alone or in combination, discloses or suggests a pipeline accelerator operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data, and to package the data and header into a message.

The Examiner admits on p. 29 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.*, to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to generate a header including information indicating a destination of data and to package the data and header into a message. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA having an address-bus/data-bus interface and lacking a message-based interface as recited in claim 22, the Examiner has failed to make a prima facie showing of obviousness.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 22.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 22 obvious.

Claims 23-24

These claims are patentable by virtue of their dependencies from claim 22.

Claim 51

Claim 51 recites receiving a message including data and information that indicates a destination of the data and processing the data with a pipeline accelerator that includes a field-programmable gate array.

In contrast, neither Dreztka nor Britton, viewed alone or in combination, discloses receiving a message including data and information that indicates a destination of data and processing the data with a pipeline accelerator that includes a field-programmable gate array.

The Examiner admits on p. 31 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.*, to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to receive a message that includes data and information indicating a destination of that data. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA that has an address-bus/data-bus interface that lacks the ability to receive a message as recited in claim 51, the Examiner has failed to make a prima facie showing of obviousness.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim

51.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to receive messages from Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 51 obvious.

Claim 52

Claim 52 is patentable by virtue of its dependency from claim 51.

Claim 53

Claim 53 recites generating with a pipeline accelerator a message header that includes a destination of data and a message that includes the header and the data.

The Examiner admits on p. 33 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.*, to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to generate a message header that includes a destination of data and a message that includes the header and the data. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA that has an address-bus/data-bus interface and that lacks the ability to generate a message header that includes a destination of data and a message that includes the header and the data as recited in claim 53, the Examiner has failed to make a prima facie showing of obviousness.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 53.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 53 obvious.

CONCLUSION

In view of the foregoing, claims 2-15, 17-24 37-47, 49-52, and 54 as previously pending and claims 1, 48, and 53 as amended are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested. **If the Examiner does not agree that all claims are in condition for allowance, the Examiner is respectfully requested to telephone the undersigned prior to issuing an action rejecting the claims to schedule a telephone interview.**

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

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